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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/041,671
Filing Date	January 10, 2002
First Named Inventor	Allon ADIR
Group Art Unit	2123
Examiner Name	
Attorney Docket Number	ADIR=2

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
	AA	6,285,974	B1	MANDYMAN et al.	09-04-2001	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
/S.P./	AB	A. SAHA et al., "A Stimulation-Based Approach to Architectural Verification of Multiprocessor System", IEEE, 1995, pp. 34-37	
/S.P./	AC	A. CHANDRA et al., "AVPGEN - A Test Generator for Architecture Verification", IEEE Transactions on Very Large Scale Integration (VLSI), June 1995, pp. 188-200, vol. 3, no. 2	
/S.P./	AD	Y. LICHTENSTEIN et al., "Model Based Test Generation for Processor Verification", Sixth Innovative Applications of Artificial Intelligence Conference, August 1994, pp. 83-94	
/S.P./	AE	B. O'KRAFKA et al., "MPTG: A Portable Test Generator for Cache-Coherent Multiprocessors", IEEE, 1995, pp. 38-44	
/S.P./	AF	Genesys - MP, User's Guide, Chapter 1-4, pp. 5-53, 1999	

Examiner Signature	/Shambhavi Patel/
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Date Considered	12/06/2008
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